Amendments to the Specification:

Please replace the paragraph beginning at page 2, line 14, with the following redlined paragraph:

More particularly, a binary ~~encoder~~ decoder is provided that, in one embodiment, includes a first pair of parallel-coupled transistors and a second pair of parallel-coupled transistors, the first and second pair of parallel-coupled transistors coupled between a voltage source and first and second outputs, respectively; a third transistor coupled between the first output and a reference potential: a fourth transistor coupled between the second output and the reference potential; and the first output coupled to a first input of the second pair of parallel-coupled transistors, the second output coupled to a first input of the second pair of parallel-coupled transistors, the first and second pair of parallel-coupled transistors each having an input terminal, and the third and fourth transistors each having an input terminal.

Please replace the paragraph beginning at page 2, line 24, with the following redlined paragraph:

In accordance with another aspect of the invention, an ~~encoder~~ decoder for integrated circuits is provided that includes a first set of parallel-coupled transistors coupled between a voltage source and a first output and comprising first, second, and third transistors each having respective inputs; a second set of parallel-coupled transistors coupled between the voltage source and a second output and comprising fourth, fifth, and sixth transistors each having respective inputs; a seventh transistor coupled between the first output and a common node and having an input: an eighth transistor coupled between the second output and the common node and having an input: and a ninth transistor coupled between the common node and a voltage reference and having an input.